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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,590	05/16/2001	Shinji Fukasawa	010623	1417

23850 7590 07/21/2003

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EXAMINER	
QUACH, TUAN N	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,590	FUKASAWA, SHINJI	
	Examiner	Art Unit	
	Tuan Quach	2814	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 19-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 19-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7, 19, 26, 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Tottori or Buynoski.

Tottori teaches mutiple wiring structure including stack via V1, V2, between wiring 21 and 23, and partitioned intermediate metal layers 22, 32, 22. See Fig. 1, column 5 line 20-58.

Buynoski shows the connection between metal 1 and metal 3 employing vias 1 and 2 and intermediate metal 2 having partitioned layers. See Fig. 1, column 5 line 45-58.

Claims 20, 21 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Tottori or Buynoski.

The product by process claims are anticipated by or otherwise obvious over the references as applied above; additionally, such automatic wiring program e.g., EDA tools, is well known in the art as acknowledged by applicant on page 1-3 of the specification.

Claims 3-6, 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tottori or Buynoski taken with Ono.

Although the references as applied above do not recite the priority direction for the intermediate layer, such selection would have been as evidenced by Ono,[0010]-[0015] wherein effective use of wiring resource of metal wiring layers can be obtained. The employment of array configuration and the deletion where appropriate would have been obvious and would have been within the purview of one skilled in the art where the pattern is not desired and where multiple levels are obtained.

Claims 8-10, 27-29 are are rejected under 35 U.S.C. 103(a) as being unpatentable over Tottori or Buynoski.

Regarding the layer to be connected being polysilicon or diffusion layer, such would have been conventional and obvious when the connection is being made to device components employing such material, e.g., polysilicon gate, and diffusion region for source/drain well known in the art, and as shown in Tottori, Fig. 1 column 5 line 14 and as such would have been obvious.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Torii teaches semiconductor intergrated circuit including automatic wiring design.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Quach whose telephone number is 703-308-1096. The examiner can normally be reached on M - F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Wael Fahmy can be reached on (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318 (Before Final) and (703) 872-9319 (After Final).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan Quach
Primary Examiner